IN THE CLAIM:

1 - 5 (Cancelled)

6. (Previously Presented) A chip module, comprising:

a chip carrier comprising a substrate formed by a carrier film and connection leads arranged on the substrate, said connection leads comprising stripes and extend parallel over the substrate, said connection leads comprising electrically conductive connection strands arranged on said substrate in a single plane and extending in a planar direction over the entire substrate surface and having a longitudinal expansion flush with the substrate surface, said electrically conductive connection strands being independent and separate elements from said substrate; and

connecting surfaces with elevated contact metallizations, said contact metallizations being in contact with a top side of said connection strands facing away from the carrier film.

7. (Previously Presented) A chip module according to claim 6, wherein the connection strands are in contact with the contact metallizations of the chip and are connected with the terminals of a coil unit.

8 - 17. (Canceled)

18. (Previously Presented) A chip carrier arrangement in accordance with claim 6,

wherein:

said carrier film and said electrically conductive strands have a flexibility to be provided in rolls.

19. (Cancelled)

20. (Currently Amended) A chip carrier arrangement formed by the process steps comprising:

providing a carrier film having a longitudinal dimension;

providing a plurality of electrically conductive connection strands, said electrically conductive connection strands being provided separately and independently from said carrier film;

attaching said electrically conductive connection strands onto said carrier film as stripes extending substantially in parallel over said carrier film, said electrically conductive connection strands being arranged on said carrier film in a substantially single plane and extending in a planar direction over said entire longitudinal dimension of said carrier film;

dividing said carrier film with attached said electrically conductive strands into a plurality of substrates, said dividing being transverse to said longitudinal dimension.

21. (Cancelled)

22. (Previously Presented) A chip carrier arrangement in accordance with claim 20, further comprising:

providing a chip with contact metallizations;

connecting said contact metallizations with said electrically conductive strands.

23. (Cancelled)

24. (Previously Presented) A chip carrier arrangement in accordance with claim 20, wherein:

said carrier film and said electrically conductive strands have a flexibility to be wound into rolls.

25. (Previously Presented) A chip carrier arrangement in accordance with claim 20, wherein:

said carrier film and attached said electrically conductive strands have a flexibility to be wound into a roll.

26. (Previously Presented) A chip carrier arrangement in accordance with claim 20, wherein:

said attaching of said electrically conductive connection strands onto said carrier film is performed with adhesive.

27. (Currently Amended) A chip carrier arrangement in accordance with claim ~~23~~ 28, wherein:

said attaching of said electrically conductive connection strands onto said carrier film is performed with adhesive;

said carrier film and attached said electrically conductive strands have a flexibility to be wound into a roll.

28. (New) A chip carrier arrangement formed by the process steps comprising:

providing a carrier film having a longitudinal dimension;

providing a plurality of electrically conductive connection strands, said electrically conductive connection strands being provided separately and independently from said carrier film;

attaching said electrically conductive connection strands onto said carrier film as stripes extending substantially in parallel over said carrier film, said electrically conductive connection strands being arranged on said carrier film in a substantially single plane and extending in a planar direction over said entire longitudinal dimension of said carrier film;

providing a plurality of chips with contact metallizations;

connecting said contact metallizations of said plurality of chips with said electrically conductive strands;

dividing said carrier film with attached said electrically conductive strands and attached said chips into a plurality of substrates, said dividing being transverse to said longitudinal

dimension, said dividing being performed to place one of said plurality of chips on each of said plurality of substrates.